Serial No. 10/501,530
Appeal Brief

Docket PD020002
Customer No. 24498

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Reiner Noske	Confirmation No.	4383
Serial No: 10/501,530	Group Art Unit:	2621
Filed: 7/14/2004	Examiner:	Torrente, Richard T
For: Method for Storing Video Signals	Atty Docket:	PD020002
		THOM:0135

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APPEAL BRIEF PURSUANT
TO 37 C.F.R. §§ 41.31 AND 41.37

This Appeal Brief is being filed in response to the Final Office Action mailed on February 27, 2009, and in furtherance of a Notice of Appeal filed May 18, 2009.

CERTIFICATE OF TRANSMISSION

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Joan Sanders

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1. REAL PARTY IN INTEREST

The real party in interest is Thomson Licensing, S.A. (hereinafter "Thomson").
Thomson has a principal place of business at 46, quai A. Le Gallo, 92100 Boulogne-
Billancourt, France. Thomson is the assignee of the present application by virtue of an
assignment dated May 6, 2004 and recorded in the U.S. Patent and Trademark Office at
reel/frame 016040/0769.

2. RELATED APPEALS AND INTERFERENCES

The Appellant is unaware of any other appeals or interferences related to this
Appeal. The undersigned is the Appellant's legal representative in this Appeal.

3. STATUS OF CLAIMS

Claims 1-5 and 8 are currently pending, are currently under rejection and, thus,
are the subject of this appeal. Claims 6, 7, and 9 have been canceled without prejudice,
and, thus, are not subject to the appeal.

4. STATUS OF AMENDMENTS

There are no outstanding amendments to be considered by the Board.

5. SUMMARY OF CLAIMED SUBJECT MATTER

The Application contains one independent claim, claim 1, which is the subject of
this Appeal. With regard to independent claim 1, discussions of the recited features can
be found at least in the below-cited locations of the specification and drawings. By way

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of example, an embodiment of claim 1 relates to a method for storing video signals (*e.g.*, provided by input 2) at a first rate (*e.g.*, CKA) and reading the stored video signals at a second rate (*e.g.*, CKB). *See* Specification, p. 1, lines 20-23; p. 6, lines 20-25; Fig. 1. The method includes compressing video signals in a first buffer memory (*e.g.*, PRE FIFO 3'). *See id.*, p. 4, l. 37-p. 5, l. 3; Fig. 1. The compressed video signals (*e.g.*, A, B, C, D) from said first buffer memory (*e.g.*, PRE FIFO 3') are stored in a random access memory (e.g., SDRAM 1), which is operated synchronously during writing and reading. *See id.*, p. 6, lines 11-18; Figs. 1 and 2. The compressed video signals (*e.g.*, A, B, C, D) are read from the random access memory (*e.g.*, SDRAM 1) into a second buffer memory (*e.g.*, FIFO 4) at the first rate (*e.g.*, CKA). *See id.*, p. 6, lines 20-22. The compressed video signals (*e.g.*, A, B, C, D) are read from the second buffer (*e.g.*, FIFO 4) at the second rate (*e.g.*, CKB) such that the compressed video signals (*e.g.*, A, B, C, D) are decompressed. *See id.*, p. 6, lines 22-25; Fig. 1.

Compressing the video signals (*e.g.*, provided by input 2) includes dividing video signals (*e.g.*, in SPLIT 3) to be stored into a plural number N of parallel data streams (*e.g.*, a, b, c, d) each carrying the inputted video signal. *See id.*, p. 4, lines 35; Fig. 1; Fig. 2. Dividing the video signal includes: delaying the parallel data streams (*e.g.*, a, b, c, d) with respect to each other by one pixel period; and time-compressing the plural number of parallel data streams (*e.g.*, a, b, c, d) to form a respective plural number of parallel time-compressed data streams (*e.g.*, A, B, C, D). *See id.*, p. 4, l. 37-p.5, l. 3; Figs. 1 and 2. Each of the time-compressed data streams (*e.g.*, A, B, C, D) is obtained by sampling every N-th pixel from the respective parallel data stream, the sampling being carried out simultaneously for the parallel data streams at the first rate. *See id.*

Storing the compressed video signals (*e.g.*, A, B, C, D) from the first buffer memory (*e.g.*, PREFIFO 3) in the random access memory (*e.g.*, SDRAM 1) includes writing the time-compressed data streams (*e.g.*, A, B, C, D) to the random access memory (*e.g.*, SDRAM 1) during a write portion of a predetermined write-read cycle of the random access memory (*e.g.*, SDRAM 1). *See id.*, p. 6, l. 36-p. 7, l. 5; Fig. 1; Fig. 3. Each of the time-compressed data streams (*e.g.*, A, B, C, D) takes up only a part of the predetermined write-read cycle. *See id.*

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Reading the compressed video signals (*e.g.*, A, B, C, D) from the random access memory (*e.g.*, SDRAM 1) into the second buffer memory (*e.g.*, FIFO 4) at the first rate (CKA) includes reading out the time-compressed data streams (*e.g.*, A, B, C, D) from the random access memory (*e.g.*, SDRAM 1) during a read portion of the write-read cycle and feeding them to the second buffer memory (*e.g.*, FIFO 4). *See id.*, p. 6, lines 20-34; p. 6, l. 36-p. 7, l. 7; Fig. 1; Fig. 3. Reading the compressed video signals (*e.g.*, A, B, C, D) from the second buffer memory (*e.g.*, FIFO 4) at the second rate (*e.g.*, CKB) includes multiplexing the decompressed data streams (*e.g.*, in MUX 5). *See id.*, Fig. 1.

6.   GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The Appellant respectfully urges the Board to review and reverse the Examiner's sole ground of rejection in which the Examiner rejected claims 1-5 and 8 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,434,625 to Willis (hereinafter "Willis") in view of U.S. Patent No. 7,034,885 to Koyanagi et al. (hereinafter "Koyanagi").

7.   ARGUMENT

As discussed in detail below, the Examiner has improperly rejected the pending claims. Further, the Examiner has misapplied long-standing and binding legal precedents and principles in rejecting the claims under 35 U.S.C. §103(a). Accordingly, the Appellant respectfully requests full and favorable consideration by the Board, as the Appellant asserts that claims 1-5 and 8 are currently in condition for allowance.

The burden of establishing a prima facie case of obviousness falls on the Examiner. *Ex parte Wolters and Kuypers*, 214 U.S.P.Q. 735 (B.P.A.I. 1979). To *establish prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 180 U.S.P.Q. 580 (C.C.P.A. 1974). Although a showing of obviousness under 35 U.S.C. § 103 does not require an express teaching, suggestion or motivation to combine prior art references, such a showing has

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been described by the Federal Circuit as providing a "helpful insight" into the obviousness inquiry. *KSR Int'l. Co. v. Teleflex, Inc.*, No. 04-1350, 550 U.S. 398, 82 U.S.P.Q.2d 1385 (2007). Moreover, obviousness cannot be established by a mere showing that each claimed element is present in the prior art. *Id.* The Examiner must cite a compelling reason why a person having ordinary skill in the art would combine known elements in order to support a proper rejection under 35 U.S.C. § 103. *Id.*

The method according to independent claim 1 recites that the video signals to be stored are divided into a "plural number N of parallel data streams each carrying said inputted video signal, whereby said dividing comprises delaying said parallel data streams with respect to each other by one pixel period." Further, claim 1 recites that the data streams are time-compressed "by sampling every N-th pixel from the respective parallel data stream, said sampling being carried out simultaneously for said parallel data streams at said first rate," and storing the compressed data streams in a random access memory. Claim 1 also recites that the compressed data streams are read out from the random access memory and multiplexed into decompressed data streams. The Appellant respectfully asserts that the division of a digital video signal into separate data streams, compressing the separated data streams by sampling every Nth pixel, storing the compressed data streams, and then multiplexing the compressed data streams after storage as generally recited in claim 1, is neither disclosed nor suggested by either Willis or Koyanagi, alone or in any hypothetical combinations.

To begin, the Examiner has alleged that Willis discloses:

> dividing video signals to be stored each into a plural number N of parallel data streams (see divided parallel stream Y_A, U_A and V_A as input to 320 in fig. 6) each carrying said inputted video signal; and time-compressing said plural number of parallel data streams to form a respective plural number of parallel time-compressed data streams (see output of 370 in fig. 6). (Final Office Action, pp. 2-3.)

However, the signals that the Examiner is citing are three analog signals, which would be inconsistent with the elements of claim 1. As stated in Willis, "the auxiliary video data is also in analog form, and Y U V format, as signals designated as Y_A, U_A, and V_A."

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Willis, Col. 14, lines 48-50. Furthermore, one of ordinary skill in the art would recognize that these are three separate data streams, each representing *a subportion* of a video signal, and are *not* generated from a single data stream. In contrast, "dividing video signals to be stored each into a plural number N of parallel data streams *each carrying said inputted video signal*," as recited by claim 1, clearly indicates that *each* video signal to be stored is divided into separate data streams, each separate data stream being identical, although delayed by one pixel. *See* Specification, p. 4, l. 32-p. 5, l. 8; Fig. 1. In fact, the present specification clearly states that in the procedure "a plurality of data streams, for example for R, G and B or Y, CR and CB, are correspondingly processed in parallel." *Id.*, p. 6, lines 1-4. Thus Willis does not disclose this element of claim 1.

Furthermore, the Examiner admits that "Willis does not disclose whereby said dividing comprises delaying said parallel data streams with respect to each other by one pixel period," but claims this is disclosed by Koyanagi (as discussed in further detail below). Final Office Action, p. 4. Thus, Willis does not disclose this additional element recited in claim 1.

Willis also does not disclose or suggest taking the divided parallel data streams and "sampling every N-th pixel from the respective parallel data stream, said sampling carried out simultaneously for said parallel data streams at said first rate," as recited in claim 1. In contrast to the allegations of the Examiner, the cited section of Willis (Col. 17, lines 44-48) merely teaches digitizing and storing each of the separate portions of the video signal. *See* Final Office Action, p. 3. Thus, Willis does not disclose this additional element of claim 1.

Further, the MUX units described in Willis are NOT "multiplexing said decompressed data streams," as recited by claim 1, but merely combine a primary and secondary chrominance signal into a single signal. (*See* Willis, Col. 20, ll. 14-20) Willis discloses synchronization of auxiliary video data with main video data by utilizing a random access memory as a field memory (350) and a first in first out line memory (354). The auxiliary video signal is delayed in the field memory and expanded in the line memory. (*See* Willis, Col. 18, lines 41-49; Fig. 6) In addition, Willis discloses various

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steps of multiplexing in Figure 8. However, the above-mentioned line memory (354) is *not* connected to one of the multiplexer "MUX" (315, 317, 319, 321, Fig. 8) but to a "DEMUX" (355) for an inverted process. Thus, Willis does not disclose this additional element of claim 1.

Koyanagi does not remedy the deficiencies of Willis, either alone or in any hypothetical combination with Willis. Koyanagi concerns an image processing circuit for interpolating between pixels to improve the resolution of an image. (*See* Koyanagi, Abstract) To perform this interpolation, Koyanagi isolates pixel values from adjoining scan lines to be used in interpolation calculations, and then interpolates between these pixels. (*See id.*, Col. 1, lines 54-67)

Koyanagi does not teach or disclose "dividing video signals to be stored each into a plural number N of parallel data streams each carrying said inputted video signal," as recited in claim 1, nor does the Examiner claim that it does. In contrast, Koyanagi is directed to extracting pixel values from adjoining scan lines. As stated in Koyanagi, "Fig. 1 is a view showing the relationship between the pixels contained in three scanning lines to be processed and four pixels generated additionally on the basis of these pixels in the image processing circuitry." (*See* Koyanagi, Col. 5, lines 53-56; Fig. 1) Thus, Koyanagi does not remedy the deficiencies of Willis with respect to this element of claim 1.

Further, in contrast to the allegations of the Examiner, Koyanagi does not disclose or suggest that the "dividing comprises *delaying* said parallel data streams with respect to each other *by one pixel period*," as recited in independent claim 1. (Emphasis added). Instead, Koyanagi uses line memories (120, 121) to delay the pixels by a period corresponding to an entire scanning line. As stated in Koyanagi, "[e]ach of the line memories 120, 121 is a first-in first-out memory for storing the pixel values of the pixels in number corresponding to one scanning line of the input signal in the input order, and *outputs the pixel value data of the input pixels at a timing delayed by one scanning line.*" Koyanagi, Col. 7, lines 63-67; Fig. 3. Thus, Koyanagi does not remedy the deficiencies of Willis with respect to this element of claim 1.

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Koyanagi also does not disclose or suggest taking the divided parallel data
streams and "sampling every N-th pixel from the respective parallel data stream, said
sampling being carried out simultaneously for said parallel data streams at said first rate,"
as recited in claim 1, nor does the Examiner claim that it does. Koyanagi does discuss
using analog sampling functions for convolution operations. *See, e.g.*, Koyanagi, Col. 14,
lines 4-15; Fig. 7. Thus, Koyanagi does not remedy the deficiencies of Willis with
respect to this element of claim 1.

In addition to the elements discussed above, Koyanagi does not disclose or
suggest "multiplexing said decompressed data streams," as recited by claim 1, nor does
the Examiner claim that it does. Indeed, Koyanagi does not mention multiplexing at all.
Thus, Koyanagi does not remedy the deficiencies of Willis with respect to this element of
claim 1.

For at least the reasons discussed above, none of the cited references, alone or in
any hypothetical combination, disclose all of the elements recited in independent claim 1.
Accordingly, claim 1 is allowable over Willis and Koyanagi. For at least the same
reasons, dependent claims 2-5 and 8 are allowable over the cited references, as well.
Accordingly, the Appellant respectfully requests the Board to reverse the rejection of
claims 1-5 and 8 under 35 U.S.C. § 103(a).

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Conclusion

The Appellant respectfully submits that all pending claims are in condition for allowance. However, if the Examiner or Board wishes to resolve any other issues by way of a telephone conference, the Examiner or Board is kindly invited to contact the undersigned attorney at the telephone number indicated below.

No fee is believed due. However, if a fee is due, please charge the additional fee to Deposit Account 07-0832.

Respectfully submitted,

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8.   APPENDIX OF CLAIMS ON APPEAL

Listing of Claims:

1.   Method for storing video signals at a first rate and reading the stored video signals at a second rate; comprising the steps of:

compressing video signals in a first buffer memory;

storing the compressed video signals from said first buffer memory in a random access memory; operated synchronously during writing and reading;

reading said compressed video signals from said random access memory into a second buffer memory at said a first rate;

reading said compressed video signals from said second buffer at said second rate such that said compressed video signals are decompressed.

wherein the step of compressing video signals includes:

dividing video signals to be stored each into a plural number N of parallel data streams each carrying said inputted video signal, whereby said dividing comprises delaying said parallel data streams with respect to each other by one pixel period; and

time-compressing said plural number of parallel data streams to form a respective plural number of parallel time-compressed data streams.

whereby each of said time-compressed data streams is obtained by sampling every N-th pixel from the respective parallel data stream, said sampling being carried out simultaneously for said parallel data streams at said first rate;

wherein the step of storing said compressed video signals from said first buffer memory in said random access memory includes:

writing said time-compressed data streams to said random access memory during a write portion of a predetermined write-read cycle of said random access memory;

whereby each of said time-compressed data streams takes up only a part of said predetermined write-read cycle:

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wherein the step of reading said compressed video signals from said random
     access memory into said second buffer memory at said first rate includes:
reading out said time-compressed data streams from said random access memory
     in a read portion of said write-read cycle and feeding them to said second
     buffer memory;
and wherein the step of reading said compressed video signals from said second
     buffer memory at said second rate includes:
multiplexing said decompressed data streams.

2.   The method according to Claim 1, wherein the write-read cycle of said random access memory a write period and at least one read period.

3.   The method according to Claim 2, wherein the write-read cycle of said random access memory comprises a write period and three read periods.

4.   The method according to Claim 2, wherein the write or read periods in each case contain, prior to the writing or reading, respectively. control time segments for setting said random access memory for writing or reading, respectively, and, after the write or read periods, respectively, control time segments for terminating the writing or reading, respectively.

5.   The method according to Claim 4, wherein said random access memory is further more refreshed in said time segments.

8.   The method according to Claim 1, wherein the video signals are divided pixel by pixel.

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9.   EVIDENCE APPENDIX

None.

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10.   RELATED PROCEEDINGS APPENDIX

None.